AMENDMENTS TO THE DRAWINGS:

Subject to the approval of the Examiner, Applicant proposes to amend FIG. 3 to redraw NP21 as an npn transistor; to relabel reference characters PN11-PN1n as NP11-NP1n, respectively; and to drawn PN11 and NP21 as npn transistors instead of pnp transistors. Applicant also proposes to amend FIG. 6 to change reference characters P1 and P2, to P61 and P62, respectively. These changes are indicated on drawing Replacement Sheets (3/6 and 6/6) attached hereto.

Attachments: Replacement Sheet 3/6 including FIG. 3 (1 page);
Replacement Sheet 6/6 including FIG. 6 (1 page).

REMARKS

In the Office Action, the Examiner objected to the drawings due to informalities and alleged errors; objected to the specification due to informalities; and objected to claims 4-7, 9, and 10 due to informalities. The Examiner also rejected claims 1-11 under 35 U.S.C. § 112, second paragraph, as being indefinite; rejected claims 1-3 and 7-9 under 35 U.S.C. § 102(b) as being anticipated by Applicant's alleged admitted prior art (hereafter "AAPA"); and rejected claims 1-3 under 35 U.S.C. § 102(e) as being anticipated by Coady (U.S. Patent No. 6,765,431 B1). The Examiner indicated that claims 4, 5, 6, 9, 10, and 11 are drawn to allowable subject matter, and would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112, second paragraph, and to incorporate any applicable limitations from their corresponding independent claims.

Applicant proposed to amend FIGS. 3 and 6, has amended the specification, and has amended claims 1 and 3-11. Claims 1-11 are pending.

Applicant gratefully acknowledges the Examiner's indication of allowable subject matter in claims 4-6 and 9-11.

Applicant has amended the specification at pages 3 and 5-12 as suggested by the Examiner in the Office Action at pages 4-5. The amendments to the specification at pages 5-12 reflect the amended language of the claims. In addition, Applicant has submitted a replacement Abstract as suggested by the Examiner at page 4 of the Office Action. Accordingly, Applicant respectfully requests that the objection to the specification be withdrawn.

The Examiner objected to claims 4-7 and 9-11 due to informalities. Applicant has amended these claims as suggested by the Examiner, and thus, respectfully requests that the Examiner withdraw the objection to claims 4-7 and 9-11, as well.

The Examiner also objected to FIGS. 3, 5, and 6. In response to and subject to the approval of the Examiner, Applicant proposes to amend FIG. 3 to redraw NP21 as an npn transistor; to relabel reference characters PN11-PN1n as NP11-NP1n, respectively; and to drawn PN11 and NP21 as npn transistors instead of pnp transistors. Applicant also proposes to amend FIG. 6 to change reference characters P1 and P2, to P61 and P62, respectively. These changes are indicated on drawing Replacement Sheets (3/6 and 6/6) attached hereto.

Support for the proposed amendments to the FIG. 3 can be found in the specification, for example, at page 14, lines 3-7. In addition, the proposed amendment to FIG. 6 is consistent with the Examiner's comments at page 2 of the Office Action. With respect to the Examiner's objection to FIG. 5, Applicant respectfully submits that given the above discussed amendments to FIG. 3, FIGS. 3 and 5 are consistent with one another. The Examiner's objection to the drawings is thus rendered moot. Accordingly, Applicant respectfully requests that the Examiner withdraw the objection to the drawings.

Applicant has amended independent claims 1 and 3 to recite "a constant voltage independent of temperature and substantially independent of the number of said plurality of first bipolar transistors and the number of said plurality of second bipolar transistors," (emphasis added). Applicant has also amended claims 7 and 8 to recite "a second connection point to one of said two resistors has a constant voltage that is

substantially independent of the number of said plurality of first bipolar transistors and the number of said plurality of second bipolar transistors." Support for these changes can be found for example, at pages 16, lines 5-20, and in FIGS. 1-3, which show VOUT.

The Examiner rejected claims 1-11 under 35 U.S.C. § 112, second paragraph. To the extent the Examiner's rejection is understood,[1] Applicant has amended claims 1 and 3-11 in light of the Examiner's comments at pages 6-8 of the Office Action. Applicant's amendments are discussed below.

1) At page 6 of the Office Action, the Examiner alleged that the phrase "a larger emitter area than the first bipolar transistor," recited in the claims 1 and 3 is unclear. Applicant has amend claims 1 and 3 to more clearly define the respective emitter areas of the "plurality of first bipolar transistors," and the "plurality of second bipolar transistors."
2) The Examiner further rejected claims 4 and 7 allegedly because the phrase "a larger emitter area than the first pnp transistor" is unclear. See Office Action at page 6. Applicant has amended claims 4 and 7 to more clearly define the respective areas of the "plurality of first pnp transistors," and the "plurality of second pnp transistors."
3) The Examiner further rejected claims 5 and 8 allegedly because the phrase "a larger emitter area than the first npn transistor," is confusing. See Office Action at page 6. Applicant has amended claims 5 and 8 to

[1] Applicant was unable to determine the location of the specific language that formed the basis of the Examiner's rejections of claims 4 and 5, based on the Examiner's citations provided in the Office Action at page 6. For example, the Examiner's rejection of claim 4 cites lines 30-33. Should the Examiner maintain the rejection of claims 4 and 5, Applicant respectfully requests that the Examiner more clearly identify any allegedly objectionable language.

more clearly define the respective areas of the plurality of npn transistors recited in claim 5 and the group of npn transistors recited in claim 8.

4) The Examiner also rejected claims 4 and 5, asserting that the "claim appears to be an incomplete thought." Office Action at page 6. To the extent the Examiner's statement is understood, Applicant has amended claims 4 and 5 to recite how the transistor is connected, as suggested by the Examiner.

5) At page 6 of the Office Action, the Examiner rejected claim 7, asserting that "there is no clear relationship between the emitter and the input terminal." Accordingly, Applicant has amended claim 7 to recite "current control means including a first input terminal to which the emitter of a n-th of the first pnp transistors is connected" (emphasis added), as suggested by the Examiner.

6) The Examiner rejected dependent claims 9, 10, and 11, stating that it is not clear how the current sources recited in these claims relate to the current sources of their respective independent claims 4, 7, and 8. Office Action at page 6-7. Applicant has amended claims 9, 10, and 11, to recite first and second current sources. Support for these changes may be found in FIGS. 1-3, for example, and corresponding text in the specification.

7) The Examiner appears to reject dependent claim 11 because of alleged inconsistencies between a "first npn transistor," a "group of first npn transistors," a "second npn transistor," and a "group of second npn

transistors," recited in claims 8 and 11 (see Office Action at page 7). Applicant has amended claims 8 and 11 to further define the npn transistors as "a one of the plurality of first npn transistors," "a plurality of first npn transistors," "a one of the plurality of second npn transistors," and "a plurality of second npn transistors," (emphasis added) respectively.

8) The Examiner further rejected claim 4 allegedly due to insufficient antecedent basis for "the corresponding power source," (emphasis added) recited in the claim. Office Action at page 7. Applicant has amend claim 4 to recite "the corresponding current source," (emphasis added) to correct this oversight.

9) The Examiner rejected claims 6 and 9 allegedly due to insufficient antecedent basis for the phrase "said differential voltage generating means," recited in these claims. Office Action at page 7. Applicant has amended claims 6 and 9 to correct these minor typographical errors.

10) At page 7 of the Office Action, the Examiner rejected claim 7 due to insufficient antecedent basis for "the corresponding power source," (emphasis added) recited within the claim. Accordingly, Applicant has amended claim 7 to correct this minor typographical error and to recite "the corresponding current source."

11) The Examiner rejected claim 10 allegedly for "being incomplete for omitting essential structural cooperative relationships of the elements." See Office Action at pages 7-8. Applicant has therefore amended claim 10 to recite "another current source that supplies a current to said

differential pair," (emphasis added) to more appropriately define the present invention.

Accordingly, in light of the foregoing, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection under 35 U.S.C. § 112, second paragraph.

Applicant respectfully traverses the rejection of claims 1-3, 7, and 8 under 35 U.S.C. § 102(b) as being anticipated by AAPA. In order to support a rejection under 35 U.S.C. § 102, each and every element of each of the claim in issue must be found, either expressly described or under principles of inherency, in that single reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q. 2d 1913, 1920 (Fed. Cir. 1989). Applicant respectfully traverses the rejection, as the AAPA does not teach at least a "voltage amplification adding means . . [including an] adding the amplified voltage to the base emitter voltage of one of said plurality of second bipolar transistors to output a constant voltage," (emphasis added) as recited in claim 1, for example.

As described in the specification at page 2, line 16-page 3, line 20, the circuits taught by AAPA, and shown in FIGS. 5 and 6, disclose an output voltage VOUT based on a sum of the "potential difference ΔVBE . . . per stage," each stage being one of n bipolar transistors. The output voltage, VOUT, is then scaled by 1/n to obtain 1.2V.

Thus, AAPA teaches an output voltage based on a sum of potential differences, but does not describe generating an output by adding a voltage to the base emitter voltage of one transistor. Accordingly, AAPA necessarily fails to teach "adding the

amplified voltage to the base emitter voltage of one of said plurality of second bipolar transistors to output a constant voltage" (emphasis added), as recited in claim 1. Claim 1 is allowable over AAPA for at least this reason.

Claim 3 recites a "voltage amplification adding means including a differential amplifier . . . to output a constant voltage . . . substantially independent of the number of said plurality of first bipolar transistors and the number of said plurality of second bipolar transistors." As discussed above, AAPA discloses an output voltage VOUT based on a sum of the "potential difference ΔVBE . . . per stage," each stage being one of n bipolar transistors. Accordingly, AAPA does not teach a "constant voltage . . . substantially independent of the number of said plurality of first bipolar transistors and the number of said plurality of second bipolar transistors," (emphasis added). AAPA therefore also does not teach each and every element recited in claim 3, and accordingly claim 3 is not anticipated by AAPA for at least this reason.

In addition, amended claims 7 and 8, though of different scope, recite similar limitations to amended claim 3, and are also allowable for the reasons discussed above with respect to amended claim 3. Accordingly, Applicant respectfully submits that claims 1, 3, 7, and 8 are not anticipated by AAPA for at least the above discussed reasons, and claim 2 is allowable at least due to its dependence from claim 1. In view of the foregoing, Applicant respectfully requests that the Examiner reconsider and withdraw the under 35 U.S.C. § 102(b).

Applicant respectfully traverses the rejection of claims 1-3 under 35 U.S.C. § 102(e) as being anticipated by Coady. Coady teaches, at column 6, lines 6-13, an output voltage, VGB which "includes the VBE of two transistors, namely transistors Q3

and Q4 . . . [t]he net result is that the bandgap reference output voltage is doubled." *Id.* Since two transistors, Q3 and Q4, are provided, VGB is twice what it would otherwise be if only one transistor were included. Thus, VGB is dependent on the number of transistors and cannot correspond to the claimed constant voltage. Coady, therefore, fails to teach a "constant voltage . . . substantially independent of the number of said plurality of transistors," as recited in amended claims 1 and 3.

Independent claims 1 and 3 are thus allowable over Coady, and claim 2 is also allowable at least due to its dependence from claim 1. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection under 35 U.S.C. § 102(e) as being anticipated by Coady.

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: June 9, 2005

By: Reg. No. 54,731
for John M. Romary
Reg. No. 26,331

Attachments: Drawing Replacement Sheets 3/6 and 6/6 (2 pages);
Replacement Abstract (1 page).

ABSTRACT OF THE DISCLOSURE

A constant voltage generating circuit which uses a band gap reference circuit to produce a constant voltage and which is effective at reducing driving voltage and noise. The voltage generating circuit has a plurality of first bipolar transistors including n first bipolar transistors, each having an emitter area. The voltage generating circuit also includes a plurality of second bipolar transistors including n second bipolar transistors. Each of the n second bipolar transistors has an associated emitter area greater than the emitter area of each of the plurality of the first bipolar transistors. The constant voltage generating circuit produces a constant output voltage that is independent of temperature and the number of first and second transistors.